



METHOD OF ANALYZING ELECTROMAGNETIC INTERFERENCE

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The present invention relates to a method of analyzing electromagnetic interference (EMI) (hereinafter often referred to as an "EMI analysis method"), and more particularly, to a method of analyzing electromagnetic interference arising in a large-scale, high-speed LSI (large-scale integrated circuit) by means of high-speed, highly-accurate logic simulation.

10 2. Description of the related Art

LSIs ~~find~~are used in a broadening range of applications, from communications devices, such as cellular phones, to general household products, toys, and automobiles, as well as applications in the field of computers. Electromagnetic interference arising in such ~~a~~ products induces radio 15 interference noise in a nearby RF receiver, such as a TV set or a radio, or in faulty operations of another nearby system. In order to prevent this problem, the ~~entirety of a whole~~ product is shielded, or filters are provided in ~~a~~ the product. With a view towards preventing an In order to reduce the need to increase in the number of components complexity and cost of production and to 20 reduce the difficulty difficulties encountered in conventional methods of preventing occurrence of electromagnetic interference in a product, strong demand exists for a means of suppression of noise in an LSI itself.

Under such a situation, ~~a~~An LSI is ranked as a key device for component of any product in which contains an LSI it is used. Demand exists for an

larger-scale, high-speed LSI for ensuring in order to ensure the competitiveness of a product. In a situation in which the cycle of As product development cycles becomes become shorter, design-automation of an LSIs is has become indispensable for satisfying the demand. There is a growing necessity need for 5 adopting synchronous circuitry in LSIs as a condition for introducing a in order to take advantage of state-of-the-art design-automation methods. In a case where When all of the circuits of a large-scale, high-speed LSI operate synchronously with a reference clock signal, instantaneously-changing current becomes very large and induces resulting in an increase in the induction of 10 electromagnetic interference.

The present invention relates to a simulation method which that enables evaluation of EMI indispensable for reducing electromagnetic interference while maintaining a tendency toward a larger-scale, higher-speed LSI.

Noise imposed on another device by an LSI is roughly classified into two 15 types; radiation noise, and conduction noise. Radiation noise emanated directly from an LSI includes noise emitted from internal wires of an LSI. However, the internal wires do are not act as an antenna of large size enough to act as an effective antenna. As operating frequencies of LSIs continue to increase, a matter of course, it is considered expected that the radiation noise emitted directly from an LSI will pose a problem in the future, in association 20 with an improvement in the operation frequency of an LSI. However, as of now, the noise emitted from the inside of an LSI is considered trivial.

In contrast, conduction noise from an LSI affects another devices mounted on a the same printed circuit board, by way of direct interconnections, such as wires external leads of an the LSI or routings traces provided on a the printed wiring circuit board. Noise is emitted from such interconnections 5 while The interconnections are act as the source of origination or as an antenna for emitting conduction noise. The antenna constituted of the interconnections is much larger than that constituted by internal wires of an LSI and is a dominant element in terms of electromagnetic emission.

A power line and a signal line can act as paths along which conduction 10 noise developing in an LSI travels. In consideration of When analyzing an electromagnetic field in the vicinity of an LSI, noise which results from variation in an electric current of a power source being emitted from a power line serving as an antenna is considered to be dominant. There may be a In some cases where ringing and overshoot phenomena stemming from variation 15 in a signal may also pose problems. However, there more frequently arises a case where variation in an internal power level of an LSI that propagates as a signal waveform, to thereby more often presents a problem. Noise emitted from a power line or a signal line is considered to have a strong correlation with variation in the electric current of a power source (hereinafter referred to as a 20 "source current").

A source current of a CMOS circuit will now be described by reference to a simple inverter circuit. In a case where When variation arises in a voltage applied to an inverter circuit, there flows a load capacity charge/discharge current flows, which is the primary source current of the CMOS circuit. In

addition, a short circuit current flows together with the load capacity charge/discharge current. In automated design of such a CMOS circuit, all circuits of an LSI are synchronized in accordance with the constraints on the use of a the design-automation tool. As a result of all circuits being 5 synchronized, all circuits of the LSI operate simultaneously, and a peak current arises in a power source in synchronism with a reference clock signal. Further, in order to increase operating speed, or shorten a cycle, of the LSI, the capacity of a transistor is increased so as to enable a charging/discharging operation to be completed within a shorter period of time. Eventually, a peak current 10 increases. As a matter of courseNecessarily, the total source current of an LSI is increased when the integration level of an LSI is increased. Thus, the peak current of the power source is increased, thereby inducing occurrence of an abrupt change in a source current. Such an abrupt change induces an increase in higher harmonic components, thereby resulting in an increase in 15 electromagnetic interference.

Highly preciseHighly precise simulation of change in a source current, which may be said to the primarily account for cause of electromagnetic interference, is considered to be effective in evaluation of predicting the electromagnetic interference arising that will arise in an LSI.

20 A conventional current simulation method for effecting transistor-level current analysis, as will be described below, has conventionally been employed.

FIG. 15 is a block diagram showing the flow of processing operations pertaining to of a conventional transistor-level EMI analysis method. According to this method, on the basis of based on layout information data is

provided O1 that pertaining to describes an LSI which that is to be analyzed through use of using a transistor-level current analysis method. there is performed layout Layout parameter extraction (hereinafter referred to simply as an “LPE”) processing O3 is performed on the layout data. Subsequently, 5 there is several processing steps are performed; circuit simulation O6 regarding of a switch-level netlist; source-of-current modeling O8; a power line LPE step O10; transient analysis simulation O12; and fast Fourier transformation (hereinafter abbreviated FFT) processing O14.

Processing pertaining to each of the foregoing processing steps will now 10 be described by with reference to FIG. 15.

First, in step O3 data are is input; layout data O1 pertaining to a semiconductor integrated circuit to be subjected to EMI analysis; parameters of elements, such as transistor elements or various parasitic wiring elements (e.g., resistors and capacitors); and an LPE rule O2 for defining a form in which 15 extracted layout parameters are to be output. In accordance with the LPE rule O2, parameters of the respective elements included in the layout data O1 are calculated, whereby a netlist O4 is produced. In step O3, parasitic elements of a power source (and the ground) are not objects of extractionextracted.

In step O6 are input the netlist O4 prepared in step O3 and a test 20 pattern O5 are input. The test pattern is used for causing a the circuit being analyzed, which serves as an object of analysis, to replicate a desired logic operation. There are calculated a A load capacity charge/discharge current and a short circuit current are calculated, which correspond to the operating state of an internal circuit, thereby producing current waveform information O7

concerning about the waveform of an electric current of a transistor. The first operation of the processing pertaining to of step O6 is effected based on the assumption that the potential of a power source (and that of ground) is a variation-free, ideal potential.

5 In step O8 is entered the current waveform information O7 concerning of a transistor prepared in step O6 is entered. The thus entered current waveform information O7 is modeled into a mode which can be applied to subsequent step O12, wherewith used to prepare current source element model information O9 is prepared suitable for subsequent step O12. In order to
10 alleviate a reduce the processing load which would be imposed on for subsequent step O12, a function circuit block consisting of a plurality of transistors is usually modeled as a single current-source element.

15 The Processing processing pertaining to performed in step O10 differs from processing pertaining to step O3, only in that rather than parameters of transistor elements and those of various parasitic wiring elements, parameters of parasitic elements of a power source and those of a ground wire (e.g., resistors, decoupling capacitance, and like elements) are taken as objects of extraction extracted, rather than parameters of transistor elements and of various parasitic wiring elements. Hence, repeated explanation is omitted. In
20 step O10, a power source (and ground) wiring netlist O11 is produced.

 In step O12 are entered the current source element model information O9 prepared in step O8 is entered, the power source (and ground) wiring netlist O11 prepared in step O10 is entered, and impedance O16 of a wire or a lead frame (including, resistance, capacitance, and inductance) is entered. Through

analysis of these input data carried out by a transient analysis simulator typified by SPICE, fluctuations in line voltage of a circuit to be analyzed subject circuit are calculated. Thus, there is produced a line voltage drop result O17 concerning the is produced which corresponds to thus calculated these

5 fluctuations in line voltage.

Subsequently, the processing pertaining to of step O6 is performed again. In contrast with the first operation of the processing pertaining to of step O6 having been effected which was based on the assumption that the potential of the power source (and the ground) is a fluctuation-free, ideal

10 potential, the line voltage drop result O17 prepared in step O12 is entered. The current waveform information O7 concerning for a transistor is prepared again in-with consideration of fluctuations in line voltage. Similarly, processing pertaining to of steps O8 and O12 is repeated.

Processing pertaining to steps Steps O6, O8, and O12 is effected are repeated several times in a looped manner, wherewith there is produced thereby producing a current waveform result O13 which that very highly accurately duplicates simulates fluctuations in line voltage.

In step O14, the current waveform result O13 prepared in step O12 is entered and subjected to fast Fourier transformation (hereinafter abbreviated

20 FFT) FFT processing, to thereby enable frequency spectrum analysis. There is obtained Thus, an EMI analysis result O15 is obtained.

In the conventional example, the precision of verification varies greatly according to the combination of the LPE processing O3, the power line LPE processing O10, and the source current modeling processing O8. However, a

certain level of accuracy of analysis can be expected. A transient analysis simulator typified by SPICE is used for limited to transistor-level analysis of an electric current. Hence, a limitation is imposed on the level of a circuit to be analyzed, and thus, an enormous amount of processing time is required. The 5 Since the integration level of a semiconductor integrated circuits has increased recently, and establishment of an EMI analysis method which is desired to enables high-speed analysis of an electric current on a higher level larger than a transistor level is desired.

A gate-level current analysis method has conventionally been proposed 10 as a current analysis method which that can be made faster. This gate-level current analysis method is used for analyzing power consumption. One example of a gate-level current analysis method is EMI-noise analysis which is to be effected that is performed in an ASIC design environment. The This method is described in "EMI-Noise Analysis Under ASIC Design Environment" 15 (ISPD&99, pp. 16 through 21). According to this technique, an event is acquired from the result of a gate-level simulation using a test vector, and the waveform of an electric current is estimated. The frequency of the thus-estimated current waveform is analyzed through fast using Fourier transformation FFT processing. More specifically, as shown in FIG. 16, a 20 logic simulation 104 is effected on the basis of based on a netlist 101 and a test vector 102, wherewith event information 105 is calculated. On the basis of the thus calculated Based on this event information 105 and on waveform information 103 obtained at the time of toggling, processing pertaining to for a current waveform calculation section 107 is executed, to thereby produce

producing a current waveform calculation result 108. This current waveform calculation result 108 is subjected to FFT processing 109, to thereby produce a frequency characteristic 110. The EMI-noise analysis method can effect ~~perform an EMI analysis operation faster than that performed according to the~~ 5 conventional gate-level EMI analysis method. However, use of a test vector still involves consumption of much ~~substantial~~ execution time. Therefore, the processing speed achieved by the ~~aforementioned~~ EMI-noise analysis method is not sufficiently high, and demand still exists for an increase in processing speed ~~of the faster~~ EMI-noise analysis method. ~~The with the~~ Another problem ~~The with the~~ 10 ~~aforementioned~~ EMI-noise analysis method ~~is that also encounters a problem of~~ ~~an the~~ analysis result being ~~is~~ dependent on the pattern of ~~an~~ employed ~~the~~ test vector ~~employed~~.

As mentioned above, the conventional example using the transistor-level current analysis method can be expected to yield a certain level of accuracy. 15 However, a transient analysis simulator typified by SPICE is used for ~~such a~~ transistor-level current analysis. ~~As such, A a~~ limitation is imposed on the level of a circuit to be analyzed, and an enormous amount of processing time is required. The level of a semiconductor integrated circuits has ~~recently~~ increased ~~recently~~, and ~~thus there is desired establishment of a need for an EMI~~ 20 analysis method ~~which method that~~ enables high-speed analysis of an electric current at a scale larger than ~~the scale that~~ which can be analyzed by a transistor-level simulator.

The ~~gate-level Gate-level~~ simulation using a test vector has also been proposed. However, the example conventional gate-level simulation technique

~~encounters difficulty in increasing does not sufficiently increase the speed of analysis. Since the gate-level simulation technique employs a test vector, an analysis result is dependent on the employed test pattern employed.~~

SUMMARY OF THE INVENTION

5 The present invention has been conceived to solve the drawbacks of the conventional methods and is aimed at evaluating electromagnetic interference developing in an LSI through a simulation by means of high-speed, highly-accurate analysis of a power-supply current.

10 To this end, the present invention provides a method of analyzing electromagnetic interference (an EMI analysis method). In contrast with ~~a~~~~the~~ known dynamic gate-level simulation method, the present EMI analysis method enables estimation of EMI noise, by means of calculating signal propagation of each node ~~through use of~~~~using~~ the signal propagation probability technique, and calculating variation time of each node ~~through use of~~~~using~~ "the Static 15 timing analysis technique". In short, the present invention is characterized in ~~involves~~ calculating a frequency characteristic from the relationship between toggle probability of each node and delay in each node.

More specifically, the present invention provides a method of analyzing electromagnetic interference ~~generating developing~~ in an LSI, comprising:

20 a correction step of correcting the amplitude of a current estimation waveform in each node which has been previously prepared for each change in each node, in accordance with the probability of variation in each node;

an addition step of adding current waveforms of all nodes together within a period of time corresponding to one cycle, provided that the

thus-corrected current waveform appears at a time a signal arrives at each node; and

a frequency analysis step of analyzing the frequency of the current waveform calculated in the addition step.

5 The probability of variation in each node is calculated through use of using the signal propagation probability technique. Further, the time at which a signal arrives at each node is calculated through use of using the static timing analysis technique. The time at which a signal arrives is defined so as to fall within the range between the maximum time and the minimum time, in 10 accordance with an average time, the maximum time, the minimum time, or a predetermined distribution such as a normal distribution.

Preferably, in the correction step, the amplitude of a current estimation waveform, which has been prepared for each change in each node, is corrected in accordance with the probability of variation in each node and a distribution 15 with respect to time (hereinafter called "chronological distribution").

More specifically, the probability of change in each node is calculated through use of using the signal propagation probability technique, and the chronological distribution at which a signal arrives at each node is calculated through use of using the static timing analysis technique.

20 Preferably, each node has a plurality of paths, and a current waveform is calculated in consideration of based on a case where each of the paths has a unique probability of change and signal arrival time.

Further, the present invention provides a method of analyzing electromagnetic interference developing in an LSI, the method comprising:

a waveform formation step of forming a current estimation waveform which has been prepared for each change in each node, as if the waveform randomly arises within a plurality of predetermined cycles, in accordance with the probability of change in each node and a time at which a signal arrives at 5 each node;

adding the thus-prepared current estimation waveforms of all nodes, to thereby derive a current waveform; and

analyzing the frequency of the current waveform, thereby determining a noise characteristic of EMI.

10 In other words, under the EMI analysis method according to the present invention, the probability of change in each node is calculated through use of using the signal propagation probability technique, and the result of calculation is stored as a probability at which a signal randomly changes. Further, a time at which a signal arrives at each node is calculated through use 15 of using the static timing analysis technique.

Moreover, the present invention provides a method of analyzing electromagnetic interference developing in an LSI, the method comprising:

a waveform formation step of forming a current estimation waveform which has been prepared for each change in each node, as if the waveform 20 randomly arises within a plurality of predetermined cycles, in accordance with the probability of change in each node and chronological distribution probability;

adding the thus-prepared current estimation waveforms of all nodes, to thereby derive a current waveform; and

analyzing the frequency of the current waveform, thereby determining a noise characteristic of EMI.

More specifically, the probability of change in each node is calculated through use of using the signal propagation probability technique, and the 5 result of calculation is stored as the probability of a signal changing randomly. A chronological distribution at which a signal arrives at each node is calculated through use of using the static timing analysis technique.

Preferably, each node has a plurality of paths, and a current waveform is calculated in consideration of based on a case where each of the paths has a 10 unique probability of change and signal arrival time.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic illustration for describing of the concept of the present invention;

FIG. 2 is a block diagram showing a portion of a circuit used in a first 15 embodiment of the present invention;

FIGS. 3A and 3B are graphs showing waveforms of signals arriving at the respective nodes of the cell shown in **FIG. 2**;

FIG. 4 is a block diagram showing the processing of a frequency characteristic calculation block according to a first embodiment of the present 20 invention;

FIGS. 5A to 5D are illustrations for describing showing a processing image according to the first embodiment of the present invention;

FIG. 6 is a flowchart of processing of a current waveform calculation according to the first embodiment;

FIG. 7 is a block diagram showing the processing of a frequency characteristic calculation block according to a second embodiment of the present invention;

5 **FIGS. 8A through 8D are illustrations for describing showing a processing image pertaining to the second embodiment;**

FIG. 9 is a flowchart of processing of a current waveform calculation according to the second embodiment;

FIG. 10 is a block diagram showing a portion of a circuit used in a third embodiment of the present invention;

10 **FIG. 11 is a graph showing signal waveforms of each path;**

FIG. 12 is a block diagram showing a frequency characteristic calculation block according to a third embodiment of the present invention;

FIGS. 13A through 13C are illustrations showing a processing pertaining image to the third embodiment;

15 **FIG. 14 is a flowchart of current waveform calculation processing according to the third embodiment;**

FIG. 15 is a flowchart for describing showing a known EMI analysis method; and

20 **FIG. 16 is a flowchart for describing showing a gate-level EMI dynamic analysis method of analyzing EMI dynamic at gate level.**

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An electromagnetic interference analysis method according to preferred embodiments of the present invention will now be described by with reference to

the accompanying drawings. As shown in FIG. 1, an EMI analysis method according to the present invention is characterized in comprises:

calculating the transition probability of a node from a netlist 1 and a transition probability 2, ~~through use of~~ using a propagation probability method, 5 and calculating a static delay 4 ~~through use of~~ using a static delay analysis method, to thereby derive a calculated probability/delay 5 of ~~a~~ the node;

estimating the waveform 6 of an electric current ~~on the basis of~~ based on the probability/delay 5 and information 3 concerning about the waveform of an electric signal at the time of toggling, to thereby derive a current waveform 10 estimation result 7; and

subjecting the current waveform estimation result 7 to a fast Fourier transformation (FFT) 8 (hereinafter called an "FFT"), thereby determining a frequency characteristic 9 of the waveform.

(First Embodiment)

15 A method of analyzing electromagnetic interference according to a first embodiment of the present invention will be described hereinbelow. As can be seen from a ~~The~~ schematic diagram shown in FIG. 1, ~~under shows~~ an EMI analysis method according to the present first embodiment.

20 ~~the~~ The quantity of electromagnetic interference developing in an LSI is to be analyzed ~~on the basis of~~ based on a transient probability and static delay propagation data, provided that a. A waveform shown in FIG. 3A appears in ~~at a~~ node A of a flip-flop (FF) cell and a waveform shown in FIG. 3B appears in ~~at a~~ node B of the FF cell (where FIG. 3B is an enlarged view of about 1.5 cycles of the signal designated by braces in FIG. 3A) when a clock signal CLK is input to

a circuit shown in FIG. 2 (where FIG. 3B is an enlarged view of about 1.5 cycles of the signal designated by braces in FIG. 3A). Here, the transition probability of a node is calculated from a previously-prepared netlist 1 and a transition probability 2. Further, a static delay 4 in a current estimation waveform per change is calculated. The amplitude of a current waveform is corrected in consideration of based on information 3 concerning about the waveform of an electric current arising at the time of a predetermined toggling operation. Provided that the corrected current waveform arises at a time at which a signal arrives at the respective node, the current waveforms which appear at all nodes during a period of time corresponding to one cycle are added to the current waveform (the current waveform estimation processing 6). The current waveform estimation result 7 determined through addition is subjected to the FFT processing 8, thereby determining the frequency characteristic 9 of EMI components of a circuit to be analyzed.

15 FIG. 4 is a block diagram for describing showing the overall prossecing flow of processing of the EMI analysis method according to the present first embodiment. FIGS. 5A through 5D are illustrations showing the principle underlying the processing. In a netlist 401, a circuit, which is an object the subject of the EMI analysis, is represented as circuit data. Delay information 20 405 concerning for each node is formed derived from the netlist 401 through using static delay calculation 403 (see FIG. 5A). Transition probability information 406 concerning for each node is formed derived from both the netlist 401 and input transition probability 402, through using propagation probability 404 (see FIG. 5B). In consideration of Based on a triangular

waveform whose area corresponds to the quantity of electric current derived by means of multiplying current waveform information by probability information, the average current waveform calculation means 408 derives an average current waveform 409 is formed by average current waveform calculation means 408 5 from element current waveform information 407 concerning for each node (see FIG. 5C) and the delay information 405. The thus-determined average current waveform 409 is taken used as average current waveform information (see FIG. 5D). The average current waveform information is subjected to FFT processing 410, thereby deriving frequency characteristic information 411.

10 FIG. 6 shows a flowchart of processing of performed by the average current waveform calculation means 408. The average current waveform calculation means 408 reads element current waveform information from a table (step 1250) and performs a current waveform calculation loop (step 1251). The base, W , of a triangular waveform of an instance to be processed is 15 extracted from an output slew (step 1252). The area of the triangular waveform is taken as being derived by means of multiplying $W \times \frac{h}{2}$ by transition probability per cycle, and I is taken as the value of the area of the triangular waveform. The height, h , of the triangular waveform is calculated from transition probability per $\frac{2 \times I}{W \times 1}$ cycle (step 1253), wherein “I” 20 denotes the quantity of electric current flowing in a cell of an event which is an object of processing being processed. This processing corresponds to processing performed by a triangular waveform shaping section. Until

variable “x” x changes from 0 to $W/2$, $h(c, i)$ expressed (by Eq.5) is added to $I(t+x)$ and $I(t-x)$. Further, Δt is added to variable “x” x (steps 1254 and 1255). Here, $I(t+x)$ denotes total electric current flowing through all the cells at time $t+x$, and $I(t-x)$ denotes total electric current flowing through all the cells at time $t-x$.

5 The frequency characteristic of a circuit to be analyzed subject circuit can be determined in the manner as mentioned previously, and a designer can analyze EMI which that would arise in a circuit of interest.

According to the EMI analysis method, a current waveform is modeled through an averaging operation, on the basis of based on static delay information and propagation probability information. The thus-obtained model is subjected to FFT processing, thereby analyzing EMI of a circuit. The EMI analysis method can analyze EMI components within a shorter period of time than an a known gate-level dynamic analysis method can.

15 In a case where performance of When EMI analysis for each path of a circuit is desired, static delay information concerning for each path is given.

In the present first embodiment, electric currents of all nodes in a circuit to be analyzed subject circuit are added. However, so long as if the number of nodes whose electric currents are to be added is controlled adjusted, 20 in accordance with as appropriate for the magnitude of an electric current or the frequency of probability, processing time can be shortened further.

(Second Embodiment)

Next, will be described an EMI analysis method according to a second embodiment of the present invention will be described. As represented by a

flowchart. In the second embodiment, as shown in the flowchart of FIG. 7, the present EMI analysis method is characterized in employing random current waveform estimation means 708 is used in lieu of the average current waveform calculation means 408 employed in of the first embodiment, and utilizing 5 random current waveform information is used in lieu of the average current waveform information. In other respects, the EMI analysis method according to the present embodiment is identical in configuration with that described in connection with the first embodiment.

FIG. 7 is a block diagram for describing showing the overall flow of 10 processing of the EMI analysis method according to the present second embodiment. FIGS. 8A through 8D are illustrations showing the principle underlying the processing. In a netlist 701, a circuit, which is an object the subject of EMI analysis, is represented as circuit data. Delay information 705 concerning for each node is formed derived from the netlist 701 through using 15 static delay calculation 703 (see FIG. 8A). Transition probability information 706 concerning for each node is formed derived from the netlist 701 and input transition probability 702, through using propagation probability 704 (see FIG. 8B). On the basis of Based on element current waveform information 707 concerning for each node (FIG. 8C) and operating frequency information 712, 20 random waveform estimation means 708 produces random current waveform information 709 (see FIG. 8D) within a plurality of predetermined cycles. The thus-produced random current waveform information 709 is subjected to FFT processing 710, thereby deriving frequency characteristic information 711.

FIG. 9 shows a flowchart of processing of ~~by~~ the random current waveform estimation means 708. The average current waveform estimation means 708 reads element current waveform information from a table (step 1280) and performs a current waveform calculation loop (step 1281). The average current waveform estimation means 708 performs loop processing until valuable "y" ~~the value of y (initially 1) changes from 1 to the value of reaches a given~~ frequency. (step 1282). The following processing is iterated until calculation of a current waveform is completed. A determination is made as to whether or not a random number is smaller than the value of probability (step 1283). If a random number is smaller, the base of a triangular waveform of an instance to be processed is extracted from an output slew (step 1284). At this time, the area of the triangular waveform is defined as $W \times \frac{h}{2}$, and I is the value of the area of the triangular waveform. The height "~~h~~" h of the triangular waveform is calculated by $2 \times \frac{I}{W}$ (step 1285), wherein "~~I~~" I denotes the quantity of electric current flowing in a cell of an event, which is an object ~~the subject~~ of processing. This processing corresponds to processing performed by a triangular waveform shaping section. Until variable "~~x~~" x (initially 0) changes from 0 to reaches $W/2$, $h(c, i)$ expressed (by Eq.5) is repeatedly added to $I(t+x)$ and $I(t-x)$. Further, Δt is added to variable "~~x~~" x (steps 1286 and 1287). Here, $I(t+x)$ denotes total electric current flowing through all the cells at time $t+x$, and $I(t-x)$ denotes total electric current flowing through all the cells at time $t-x$.

The frequency characteristic of a circuit to be analyzed subject circuit can be determined in the manner as mentioned previously mentioned, and a designer can analyze EMI which that would arise in a circuit of interest.

According to the present EMI analysis method, a current waveform is 5 modeled through using a random current waveform operation, on the basis of based on static delay information and propagation probability information. The thus-obtained model is subjected to FFT processing, thereby analyzing EMI of a circuit. The EMI analysis method can analyze EMI components with high accuracy within in a shorter period of time than a known gate-level dynamic 10 analysis method.

In a case where When performance of EMI analysis for each path of a circuit is desired, static delay information concerning for each path is given.

In the present-second embodiment, electric currents information of for all nodes in a circuit to be analyzed subject circuit are added. However, so long 15 as if the number of nodes whose electric currents are to be added is controlled adjusted, as appropriate for in accordance with the magnitude of an electric current or the frequency of probability, processing time can be shortened further.

(Third Embodiment)

20 An EMI analysis method according to a third embodiment of the present invention will now be described. In the previously-described first and second embodiments, delay information and probability information are prepared separately. Information is derived by means of multiplying waveform information, which is obtained as element current waveform

information, by probability information. The thus-obtained information is added to a delay time of each node. In contrast, in the present third embodiment, delay propagation probability information is ~~formed~~derived from delay propagation probability information. Delay/transition probability is 5 calculated from the delay propagation probability information, and element waveform information is added to the thus-calculated delay/transition probability.

In this way, more realistic current waveform information is calculated, and, the ~~The result of this~~ current waveform calculation is subjected to FFT 10 processing, thereby determining the frequency characteristic of an EMI component of a circuit to be analyzed. Thus, EMI of the circuit is analyzed. As can be seen from an enlarged view shown in FIG. 10, the present embodiment is directed particularly a case where a plurality of paths ~~are~~is provided in a composite cell. FIG. 11 shows delay transition information concerning 15 propagation of a signal in each of the paths of the composite cell shown in FIG. 10. FIG. 11 shows delay transition probability information as one example. As can be seen from FIG. 11, ~~there is obtained~~ node information is obtained concerning ~~for~~ a plurality of paths, and mean current waveform information is ~~formed~~derived from the node information.

20 FIG. 12 is a block diagram for ~~describing~~showing the overall flow of processing of the EMI analysis method according to the present embodiment. FIGS. 13A through 13C are illustrations showing the principle underlying the processing. FIG. 14 is a flowchart of average current waveform calculation means used in the processing. In a netlist 901, a circuit, which is ~~an object~~the

subject of EMI analysis, is represented as circuit data. Delay/transition probability 906 of each node is calculated from the netlist 901 and input transition probability 902, on the basis of ~~based on~~ delay/propagation probability 904 (see FIG. 13A). Mean current waveform estimation means 908 produces mean current waveform information 909 (see FIG. 13C), in consideration of ~~based on~~ a triangular waveform whose area is determined by the quantity of electric current, such that the delay/transition probability 906 is multiplied by element current waveform information 907 (see FIG. 13B). The thus-formed ~~calculated~~ mean current waveform information 909 is subjected to FFT processing 910 within a time domain which ~~that is determined on the basis of~~ ~~using~~ operating frequency information 912, thereby obtaining frequency characteristic information 911.

FIG. 14 shows a flowchart of processing ~~of~~ ~~by~~ the average current waveform calculation means. The average current waveform calculation means reads element current waveform information from a table (step 1310) and performs a current waveform calculation loop (step 1311). The following processing is iterated until calculation of a current waveform is completed. The delay/transition probability 906 calculated from delay information and transition probability information is multiplied by element current waveform information 907 (see FIG. 13B) (step 1312). ~~In consideration of~~ ~~Based on~~ a triangular waveform whose area is determined by the quantity of electric current, average electric current waveform estimation means 908 adds the result of multiplication as mean current, thereby deriving average current

waveform information 909. The average current waveform information 909 is subjected to FFT processing 910, thereby determining frequency characteristic information 911.

5 ~~The frequency characteristic of a circuit to be analyzed~~ subject circuit can be determined in the manner as mentioned previously, and a designer can analyze EMI, ~~which that~~ which would arise in a circuit of interest.

According to the ~~present~~ EMI analysis method, delay propagation probability information is ~~formed~~ derived from static delay information and propagation probability information, and average current waveform information is ~~formed~~ derived from the delay propagation probability information. The thus-obtained average current waveform information is subjected to FFT processing, thereby enabling highly-accurate EMI analysis.

10 ~~The EMI analysis method can analyze EMI components within a shorter period of time than ~~each~~ a known gate-level dynamic analysis method~~ can.

20 In addition to a distribution taking into consideration a path, a temperature/process/voltage distribution may be conceived as the delay/transition probability information shown in FIG. 13A.

In ~~each~~ of the foregoing embodiments, FFT processing has been used for analyzing a frequency. However, the present invention is not limited to FFT

processing. Needless to say, another processing method, such as ordinary Fourier transformation, may alternatively be employed.

5 The present invention can materialize facilitate evaluation of EMI developing in an LST-LSI through a simulation, by means of highly very accurately analyzing, through static processing, variation in power-supply current which may be said to primarily account for EMI. Further, in contrast with dynamic analysis of EMI, which is embodied by a gate-level simulation or a
10 like simulation, the present EMI analysis method can prevent an increase in processing time.